Radiation test to Study the radiation tolerance and mitigation methods of front-end readout ASIC for DAMPE Mission

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Outline

- DAMPE
- Front-End Readout ASICs
- Radiation tolerance of the ASICs
- Mitigation methods and validation
- SEL events in orbit
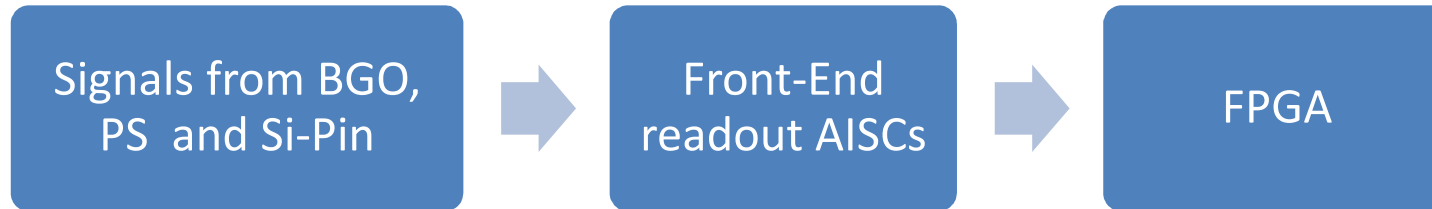
DAMPE
(Dark Matter Particle Explorer)

- Supported by the Strategic Priority Programs on Space Science, Chinese Academy of Sciences
- Lunched on December 17th, 2015
- Mission period : > 3 years
- 500Km orbit
- DAMPE payloads:
  - Plastic Scintillation Detector (PSD)
  - Silicon Tracking (STK)
  - BGO Calorimeter (BGO)
 - Neutron Detector (ND)

The DAMPE Detector

STK
(Silicon Tracker)

PSD
(Plastic Scintillation Detector)

BGO
(BGO
Calorimeter)

ND
(Neutron Detector)

Front-End Readout ASICs
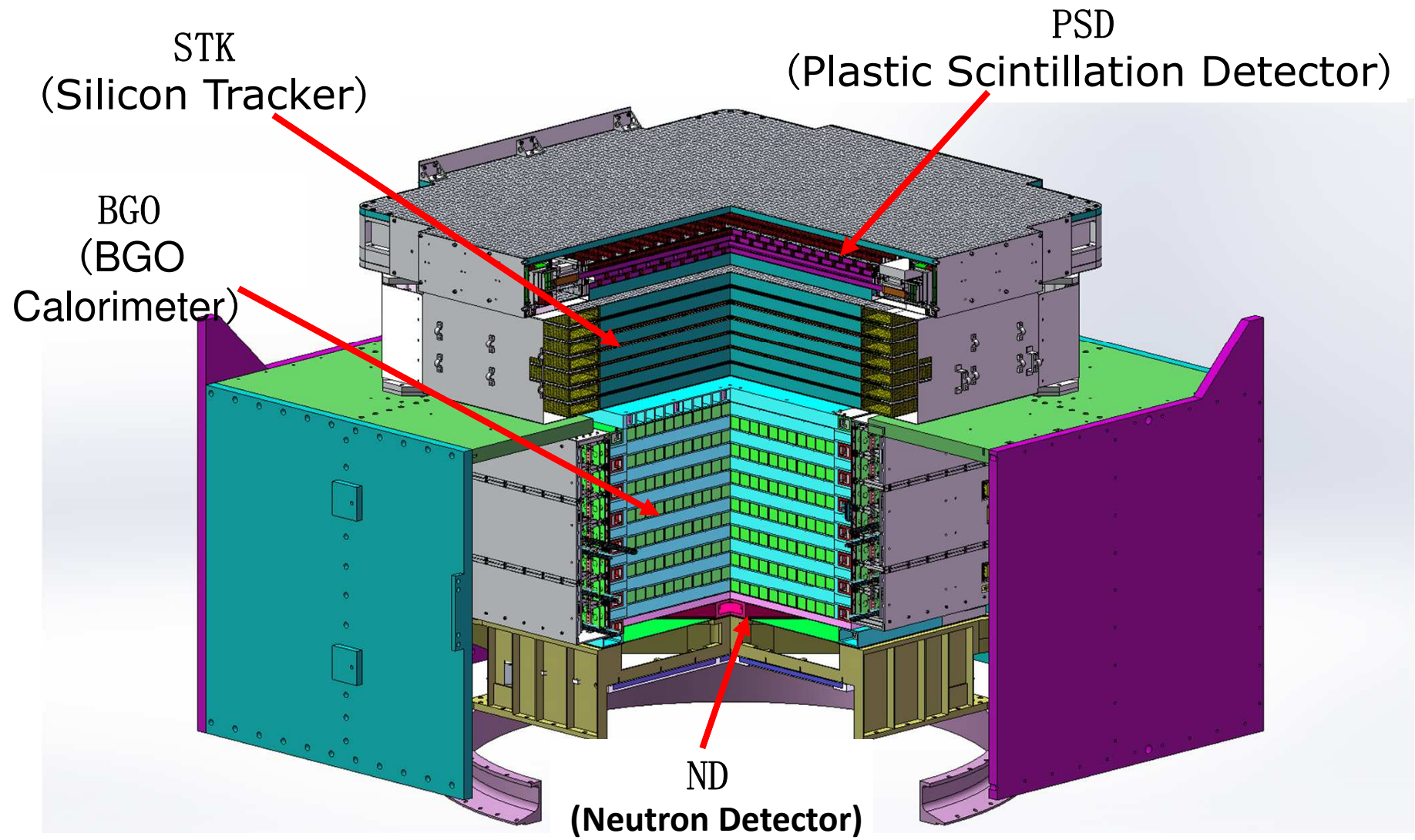

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Signals from BGO,    →    Front-End         →    FPGA
PS and Si-Pin             readout AISCs
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- VA160 and VATA160 for BGO Calorimeter
  - 52 VA160 chips, 32 VATA160 chips
- VA160 for Plastic Scintillation Detector
  - 16 VA160 chips
- VA140 for Silicon Tracker
  - 1152 VA140 chips
- Designed by IDEAS in Norway
  - Based on VA32 and TA32, modified in I/O interface
  - Fabricated by AMS in Austria, 0.35 CMOS process

Front-End Readout ASICs

- VA32: 32-channel read out in parallel/serial
- TA32: 32-channel trigger
- VATA=VA+TA
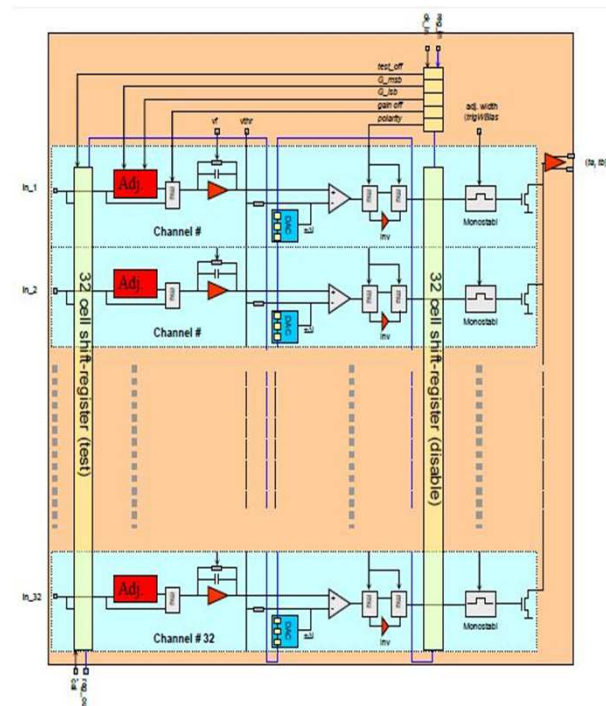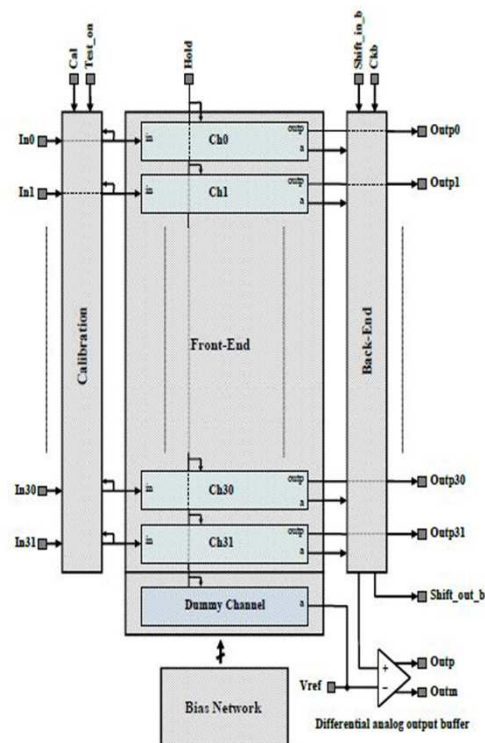
Radiation tolerance of the ASICs

- Radiation: TID SEU SEL

➤ TID: long time effect and can be shielded, test data is needed for shielding, test can be performed at any time at low cost

➤ SEU: instant effect and can be corrected using software, test data is not strongly demanded

➤ SEL: instant effect and hard damage, test date is needed for mitigation, test is expensive and not always available
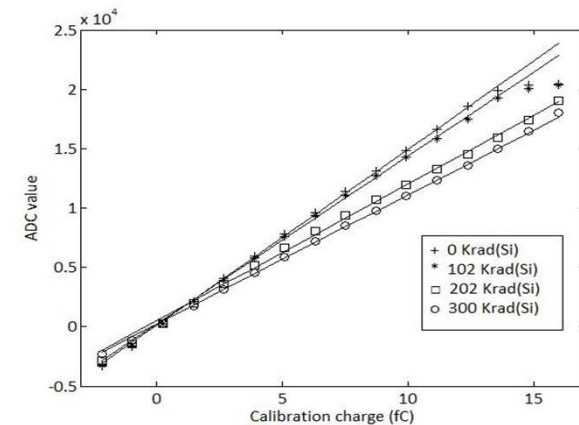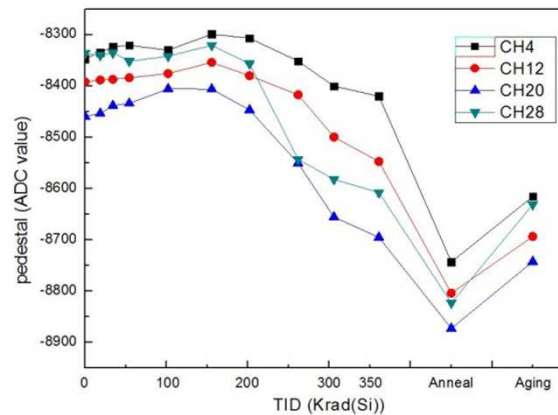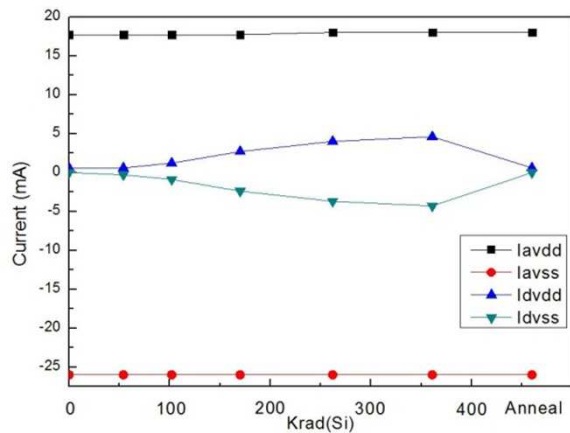
Radiation tolerance of the ASICs
SEU

- Main part of VA160, VATA160and VA140 is analog circuit, which is not sensitive to SEU

  ➢ VA: SEU risk mainly exists in the (32+32) shift registers

    ● Reset the shift registers after every trigger, which greatly reduce the SEU probability, and the errors will not be accumulated

  ➢ TA: SEU risk mainly exists in the 165 bit configuration registers

    ● TMR design is built in, the registers can detect SEU errors and correct them automatically, which greatly reduce the risk

Radiation tolerance of the ASICs
TID

- ## TID test using ^{60}Co source, in Beijing and USTC

- ## TID tests on VA32 and TA32

  ➢ Total dose up to 25.2krad(Si)

  ➢ No notable change of performance after160 hour annealing@100°C

Gao Shan-Shan, Feng Chang-Qing*, et al., Radiation tolerance studies on the VA32 ASIC for DAMPE BGO calorimeter, Nuclear Science and Techniques, 2014, 25(1)

Radiation tolerance of the ASICs

TID

- TID tests for VA160 and VATA160
  - ➢ Total dose up to 30 krad(Si)
- TID tests for VA140
  - ➢ Total dose up to 20 krad(Si)

From the TID results, the modification to VA32 does not change the TID tolerance a lot, so there maybe not much change in SEL.

Radiation tolerance of the ASICs

SEU and TID

- SEU and TID were not considered as serious problems

  ➢ SEU is a soft error that can be corrected using reset and TMR methods.

  ➢ TID is estimated to be about 3 krad(Si) for 3 years mission in a 500Km orbit, considering the shield effect of the satellite and payload structure

Radiation tolerance of the ASICs
SEL test

- More attentions were paid on SEL of ASICs
  - ➢ Hard error leading to permanent damage
  - ➢ 68 VA160 chips, 32 VATA160 chips and 1152 VA140 chips used, there maybe lot of SEL events
  - ➢ a series of SEL tests were conducted to evaluated the SEL tolerance

Radiation tolerance of the ASICs
SEL test using Laser pulse

Laser pulse tests were performed firstly to qualify the SEL sensitivity

- VA160
  - ➢latch-up occurred at the energy of 5.0-6.0nJ
  - ➢latch-up current is about 200mA(Max.)
  - ➢the sensitive location is the shift registers
- VATA160 (primary version)
  - ➢latch-up happened easily in the joint area of VA and TA and latch-up current could reach 1800mA
  - ➢the latch-up current of the TA part is about 300-400mA

Radiation tolerance of the ASICs

SEL test using Laser pulse

- VATA160 (R1)
  - ➤ Modified from the primary version of VATA160
  - ➤ No SEL event observed in the joint area
  - ➤ SEL performance of VA and TA part is still the same

From the Laser pulse test results of VA160 and VATA160, the ASICs are relative sensitive to SEL, the latch-up current is less than 500mA

SEL test using laser pulse

Radiation tolerance of the ASICs
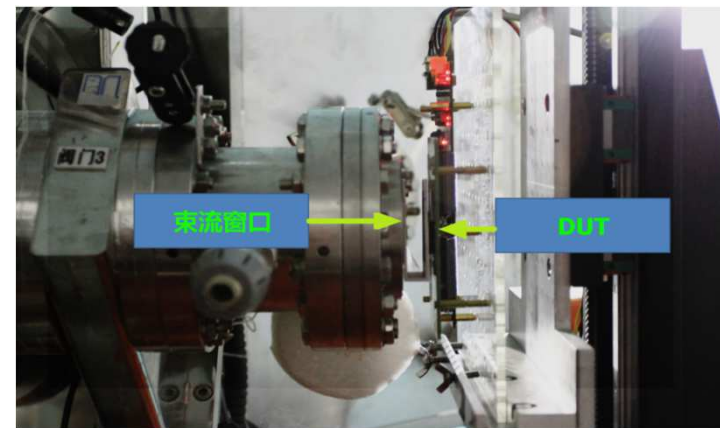## SEL test using ion beam

- Ion beam test on VA32 and TA32

    To estimate the LET of ion beam for VA140, VA160 and VATA160

    - VA32: between 22.83 and 24.77 MeV·cm^2/mg

        - accompanying with a large number of SEU

    - TA32: LET < 29 MeV·cm^2/mg, with large latch-up current

        - The gold wire bonded to DVDD pad was soon melted out, with ion beam at 29 MeV·cm^2/mg, No chance to obtain exact threshold data
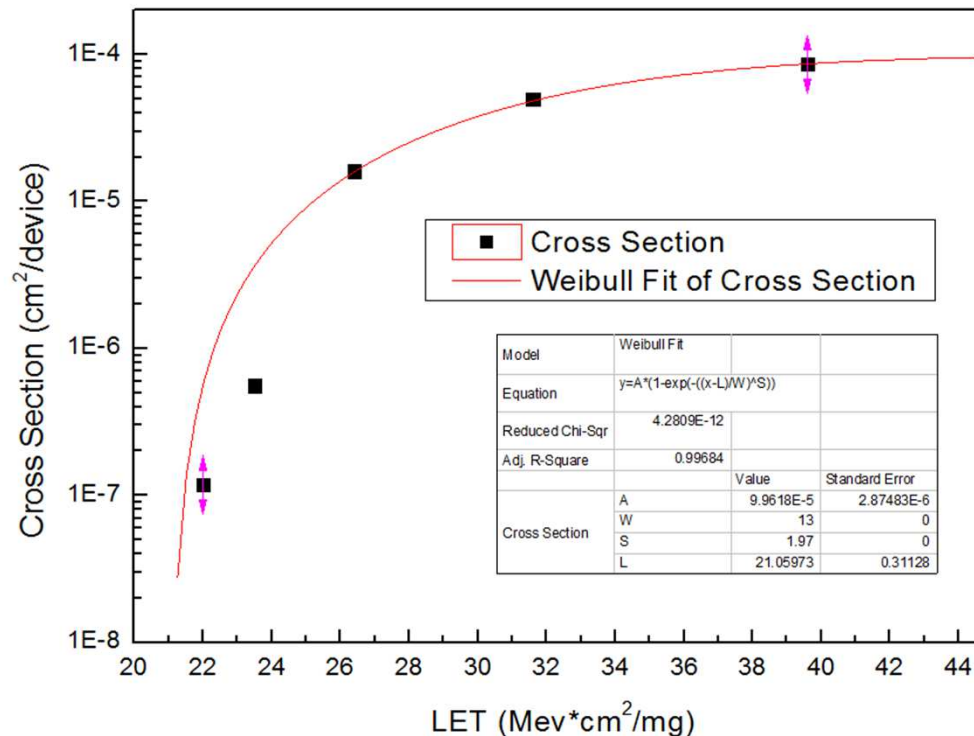

SEL experiment using ion beam

Radiation tolerance of the ASICs
SEL test using ion beam

- Ion beam test on VA160

  ➢ Threshold: 20.6～22.0 MeV*cm2/mg

  ➢ Saturated Cross Section is about 1.0×10^{-4} cm^2/device

Radiation tolerance of the ASICs
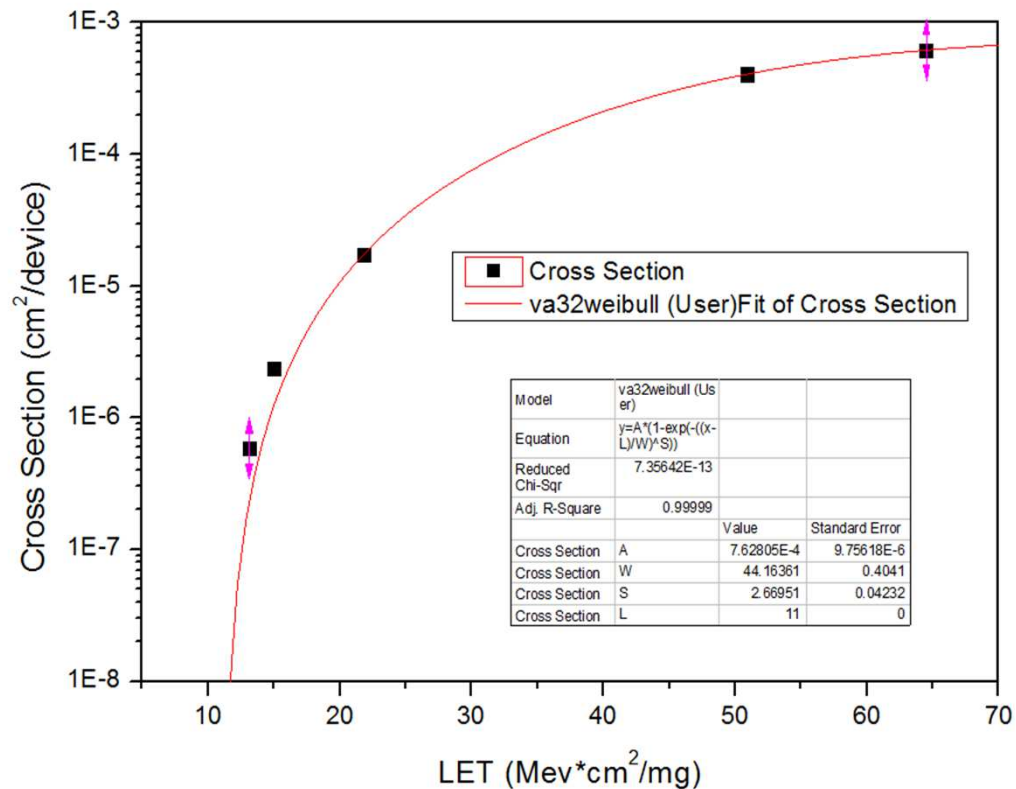## SEL test using ion beam

- Ion beam test on VATA160 (primary version)

    Lower LET limit of the ion beam: 20.6 MeV*cm^2/mg

    ➢ VA part threshold: 20.6～22.0 MeV*cm^2/mg

    ➢ TA part threshold: < 20.6 MeV*cm^2/mg, very sensitive

    ➢ The joint area of VA and TA: highly sensitive with latch-up current up to 1800mA, as in the laser pulse test

Radiation tolerance of the ASICs
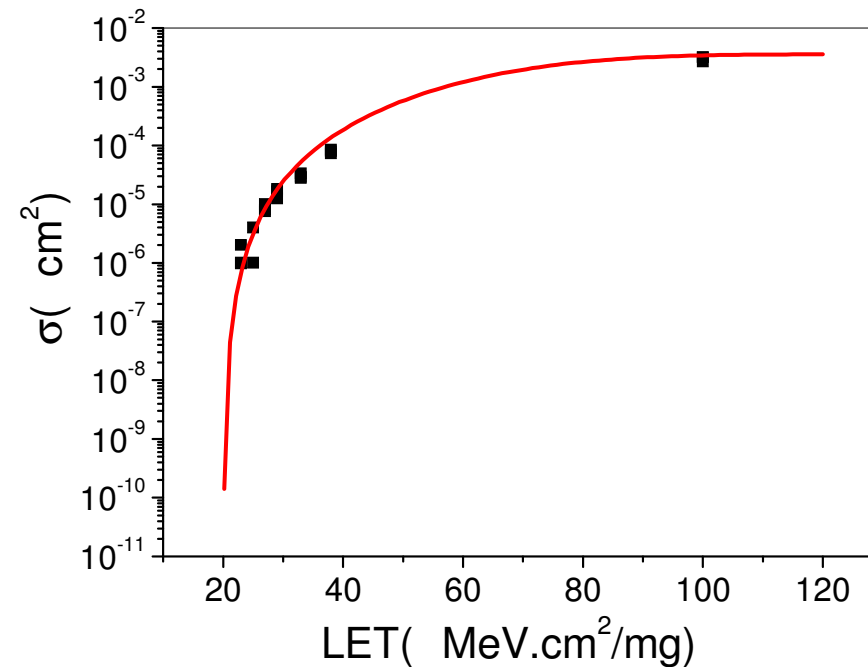## SEL test using ion beam

- Ion beam test on VATA160 (R1)
  - Threshold: about 11.0 MeV*cm^2/mg (TA part)
  - Saturated Cross Section is about 7.6×10^{-4} cm^2 (TA part)

Radiation tolerance of the ASICs
SEL test using ion beam

- Ion beam test on VA140

➢ threshold: 20 MeV*cm2/mg

➢ Saturated Cross Section: is about $3.6×10^{-3}cm^2$

Radiation tolerance of the ASICs
In orbit SEL events evaluation

- Estimated SEL events of VA

➢ VA160: saturated Cross Section is about 1.0×10^{-4} cm^2, maybe $2*10^{-5}$ events/chip/day, **nearly 0.06 events a month for 100 chips**

➢ VA140: saturated Cross Section is about 3.6×10^{-3} cm^2, maybe $4*10^{-4}$ events/chip/day, **nearly 13 events a month for 1152 chips**

Radiation tolerance of the ASICs
In orbit SEL rates evaluation

- Estimated SEL events of VATA160(TA part)

  ➢ LET Threshold: 11.0 MeV·cm^2/mg, Cross section: 7.6×10^{-4} cm^2/device

  ➢ SEL rate per chip: 8.1×10^{-5} device^{-1}*day^{-1}

  nearly 0.08 events/month for 32 chips

Overall, there maybe 0.06+0.08+13$\approx$13 SEL events a month in orbit.

SEL mitigation methods and validation

- Supply current limitation
- Automatically power off and on
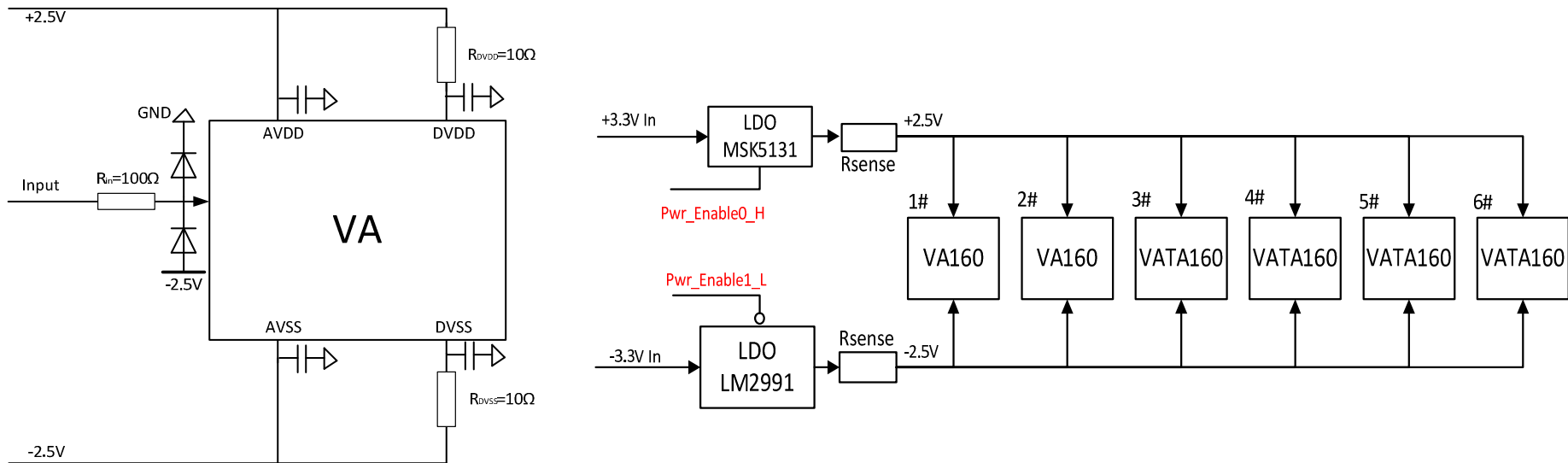
Shanshan Gao, Di Jiang, et al., Single Event Effect Hardness for the Front-end ASICs in the DAMPE Satellite BGO Calorimeter, Chinese Physics C, 2016, 40(1).

Changqing Feng, et al., Design of the Readout Electronics for the BGO Calorimeter of DAMPE Mission, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, 2015, 62(6): 3117-3125.

SEL mitigation methods and validation
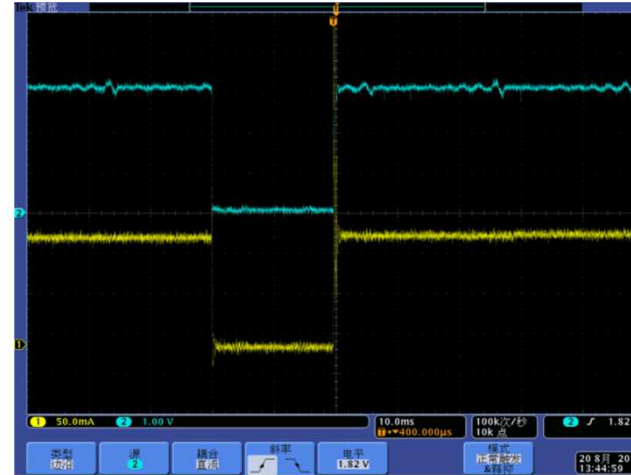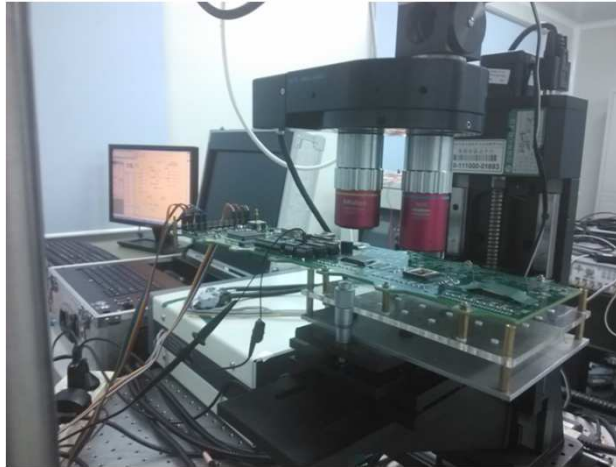
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Supply current	AVDD	DVDD	AVSS	DVSS
Before latch-up	16.4	0.00	-33.2	-0.8mA
single latch-up（no resistor）	13.9	129.6	-66.0	-95.1
Multi latch-up （no resistor）	18.0	195.6	-72.2	-153.3
Multi latch-up （no resistor）	17.6	301.8	-112.3	-216.1
Multi latch-up （**with 10 Ω resistor**）	**17.6**	**97.6**	**-64.4**	**-70.5**

SEL events in orbit

- Over current and power reset events will be recorded into the engineering data

- Nearly 3 months working in orbit, no event recorded

  ➢ inaccurate model and calculation

  ➢ the affection of shielding was not considered

  ➢ Very lucky

Scientists will give us a big surprise about our universe in the further